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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/608,315	06/26/2003	Hong Wang	42P13148	8011

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/608,315	WANG ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6,8-11,13,14,16-20,22,24-28 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-6, 8-11, 13-14, 16-20, 22, 24-28, and 30-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1-3, 5-6, 8-11, 13-14, 16-20, 22, 24-28, and 30-32 are presented for examination.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-3, 5-6, 8-11, 13-14, 16-20, 22, 24-28, and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slegel et al. (IBM's S/390 G5 Microprocessor Design).

5. Slegel substantially taught the invention of exemplary claim 8 including: "a machine-readable medium having stored thereon a sequence of instructions which when executed by a processor, cause the processor to perform a set of operations comprising: generating compiled code for a given ISA, the compiled code including a) discrete regions of microarchitecture implementation-specific code bounded by ISA

format markers and b) macroinstructions outside the discrete regions." The examiner would suggest applicants read the second paragraph on the first page of the article; the section entitled "Microarchitecture"; the section entitled "L1 cache"; and the section entitled "Millicode", at a minimum, before responding. Note that in the last paragraph of the section entitled "L1 cache" Slegel taught: "The L1 cache unit also contains a 32-byte writeable millicode array containing the millicode for the most commonly used ESA/390 instructions implemented in millicode." It is the examiners' contention that the millicode array is a microarchitecture representation of ESA/390 (macro) instructions that will also be found in the L1 cache at some point in the execution of a given program and both constitute a portion of the second code generated. (Applicants have questioned whether the examiner's contention (i.e. inherency argument) is persuasive. The examiner would direct applicants to Fig. 2 where it shows that all 390 instructions will be passing through the L1 cache as they are retrieved from the L2 cache, etc. Unless applicant can provide convincing evidence that the "most commonly used ESA/390 instructions implemented in millicode" are never used, the examiner's inherency argument stands.) Slegel inherently taught "the compiled code including a) discrete regions of microarchitecture implementation-specific code bounded by ISA format markers and b) macroinstructions outside the discrete regions." Note, in the second paragraph of the article, Slegel taught: "The G5 system implements the ESA/390 instruction-set architecture, which is based on and compatible with the original S/360 architecture introduced in 1964." While one might wish to recompile an S/360 program or at the very least optimize the compiled code for execution on the G5 system, Slegel

is saying that at least some S/360 programs could run (i.e., they are compatible) on the G5 system and could take advantage of the millicode routines in the L1 cache (i.e., there would be macroinstructions and microinstructions encompassing the same operations). Slegel also taught:generating boundary markers to mark a beginning and an end for the alternative representation, the boundary markers being in a format of the ISA (Millicode section)." The 390 macroinstruction, which is recognized by the decoder as requiring millicode, acts as one boundary and the millicode instruction that acts as a hardwired subroutine return acts as the other boundary. Applicants have not claimed a detailed definition for the terms ISA format marker/(boundary marker). Applicants' markers are nothing more than some combination of bits in the code stream which enables the processor to distinguish when it is to transition from one mode to another. Slegel clearly teaches this functionality.

6. Applicants added language to exemplary claim 8 turning the ISA format markers into "separate" ISA format markers. This language is apparently meant to distinguish over the fact that Siegel recognizes changes in the instruction encoding to tell him when there is a boundary. Slegel makes it clear (see paragraph 9, *supra*) that it is well-known by those of ordinary skill in the art how one produces both macroinstructions and microinstructions which can perform the same actions. He also makes it clear (see paragraph 9, *supra*) that it is known that both types of instructions can coexist in the same processor and that boundary markers (i.e. some combination of bits in the code stream which enables the processor to distinguish when it is to transition) are also known to those of ordinary skill. Applicants made it clear in their response to the

examiner's 112, 2nd rejection (p. 9 of applicants' Remarks filed on 10/10/2007) that a prior art compiler/(optimizing compiler) could readily be used by one of ordinary skill in the art to create applicants' compiled program "including a macroinstruction segment and microinstruction segment, the microinstruction segment representing an alternate implementation of a function of the macroinstruction segment; storing the second compiled code as a single compiled program." It is also clear compilers are capable of generating appropriate boundary markers. The examiner takes Official Notice of the fact that delimiters such as record marks, file marks, field delimiters, etc. that are separate from the data being separated are old and well-known in the art. In fact, there are over 1600 references to record marks in the USPAT and PGPUB databases going back over 30 years. As the examiner noted, it is important that some combination of bits in the code stream enable the processor to distinguish when it is to transition. Whether the design choice is something that is integral to the data stream, as Siegel taught, or somehow distinguishes itself from the normal stream, as in the case of something like a record mark, it is only important that the processor be able to recognize it.

7. To assist applicants should they chose to challenge the examiner's Official Notice, the examiner is pointing out that following the KSR decision by the Supreme Court, the Office has changed its policy related to Official Notice. The Office now requires applicants to provide persuasive evidence and/or arguments directly refuting the Official Notice before a supporting reference is to be supplied by the examiner.

8. MPEP 2141 reads, in part, as follows:

The Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), but stated that the Federal Circuit had erred by applying the teaching-suggestion-motivation (TSM) test in an overly rigid and formalistic way. *KSR*, 550 U.S. at, 82 USPQ2d at 1391. Specifically, the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "by holding that courts and patent examiners should look only to the problem the patentee was trying to solve" (*Id.* at__ 82 USPQ2d at 1397); (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem" (*Id.*); (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the combination of elements was obvious to try'" (*Id.*); and (4) by overemphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "[r]igid preventative rules that deny factfinders recourse to common sense" (*Id.*).

In *KSR*, the Supreme Court particularly emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *Id*, at__82 USPQ2d at 1395, and discussed circumstances in which a patent might be determined to be obvious. Importantly, the Supreme Court reaffirmed principles based on its precedent that "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. "*Id*, at__82 USPQ2d at 1395.

9. The Supreme Court further stated that:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his ordinary skill. *Id.* at__82 USPQ2d at 1396. When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.* at__82 USPQ2d at 1396.

10. All the elements necessary to produce the invention of applicants' claim 8 were known in the art. How one combined such elements to produce applicants' invention was also well-known in the art. One of ordinary skill would have readily recognized that the results of the combination were predictable. Absent some secondary

considerations, not in evidence at this time, applicants' invention is obvious over the combination of prior art presented.

11. As to claims 9-11, 13, and 20, see the preceding explanations related to claim 8.

12. Applicants claims 30 and 31 are representative of the substance of claims 1-3, 5-6, 8-11, 13-14, 16-20, 22, and 24-28. They are reproduced below.

> Claim 30. A method, comprising: loading a source program; compiling the source program into a first compiled code including macroinstructions for an instruction set architecture (ISA); optimizing the first compiled code into a second compiled code, the second compiled code including a macroinstruction segment, a microinstruction segment, and boundary markers, the boundary markers separate from the macroinstruction segment and the microinstruction segment, the microinstruction segment representing an alternate implementation of a function of the macroinstruction segment; storing the second compiled code as a single compiled program.
>
> Claim 31. The method of claim 30, further comprising: generating boundary markers to mark a beginning and an end of the microinstruction segment, the boundary markers being in a format of the ISA.

13. Slegel makes it clear (see the rejection related to claim 8, *supra*) that it is well-known by those of ordinary skill in the art how one produces both macroinstructions and microinstructions which can perform the same actions. He also makes it clear (see the rejection related to claim 8, *supra*) that it is known that both types of instructions can coexist in the same processor and that boundary markers are also known to those of

ordinary skill (see the rejection related to claim 8, *supra*). The examiner has made it clear that the concept of separate boundary markers is old and well-known in the art (see the rejection related to claim 8, *supra*). Applicants made it clear in their response to the examiner's 112, 2nd rejection (p. 9 of applicants' Remarks filed on 10/10/2007) that a prior art compiler/(optimizing compiler) could readily be used by one of ordinary skill in the art to create applicants' compiled program "including a macroinstruction segment and microinstruction segment, the microinstruction segment representing an alternate implementation of a function of the macroinstruction segment; storing the second compiled code as a single compiled program." It is also clear compilers are capable of generating appropriate boundary markers.

14. All the elements of claims 30-31 were known to those of ordinary skill in the art as well as how one would use compiler technology to create applicants' invention. The results of the combination are certainly predictable to one of ordinary skill in the art and must have been given applicants' arguments to overcome the examiner's 112, 1st paragraph rejection. Based on the recent KSR decision by the Supreme Court, this constitutes a *prima facie* case that applicants' invention was obvious at the time of invention.

15. Any differences between the language of claims 1-3, 5-6, 8-11, 13-14, 16-20, 22, and 24-28 and that of claims 30 and 31, does not rise to the level of patentable differentiation and represents, for the most part, semantics. The fact that the instructions are fetched and decoded as mentioned in some claims is essential/inherent to any useful system.

16. Applicants' new claim 32 merely states applicants could use unused forms of the ISA that are recognizable as boundary markers by the decoder. The concept of separate boundary markers was known in the art. Siegel taught changes in instruction encoding could signal a boundary. Logically, one of ordinary skill would recognize and could predict that some unexecutable instruction format would be separate from a macroinstruction segment and microinstruction segment and could be recognized by a decoder as a boundary marker between the two.

17. Applicant's arguments with respect to claims 1-3, 5-6, 8-11, 13-14, 16-20, 22, 24-28, and 30-32 have been considered but are moot in view of the new ground(s) of rejection.

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

19. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

20. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/William M. Treat/
Primary Examiner, Art Unit 2181